Listing of claims:

Claims 1-15 (canceled).

16. (Original) A method for testing an integrated circuit having a plurality of registers therein, each one of the registers including at least one register bit having a scan output, said method comprising the steps of:

configuring the registers to form at least one serial shift register using the scan output of each register bit;

shifting a test pattern into the at least one serial shift register;

configuring the registers in a normal mode of operation, including disabling the scan output of at least some register bits so that for each of the at least some register bits, the scan output thereof is disabled from providing a value indicative of a value maintained by the register bit; and

applying at least one clock cycle to the registers.

17. (Original) The method of claim 16, wherein the step of configuring the registers in a normal mode of operation comprises the step of driving the scan output of at least some of the register bits to a predetermined logic value.

18. (Original) The method of claim 16, further comprising repeating the steps of configuring the registers to form at least one serial shift register chain, shifting, configuring the

registers in a normal mode of operation, and applying the at least one clock cycle for different test patterns a number of times.

19. (Original) The method of claim 18, further comprising, following the step of repeating, the step of:

configuring the registers in a normal mode of operation, including disabling the scan output of the at least some register bits and driving the scan output to the predetermined logic value.

20. (Original) A method for operating a flip-flop having serial scan capabilities including a scan output, said method comprising the steps of:

receiving a mode configuration signal for configuring the flip-flop between a test mode of operation and a normal mode of operation; and

selectively disabling the scan output from providing the logic value stored by the flip-flop based upon the value of the mode configuration signal received.

21. (Original) The method of claim 20, further comprising:

selectively driving the scan output to a predetermined logic value based upon the value of the mode configuration signal received.

22. (Original) The method of claim 21, wherein the step of driving comprises driving the scan output to a low logic value.

23. (Original) The method of claim 21, wherein the step of driving comprises driving the scan output to a high logic value.

24. (Original) The flip-flop of claim 20, wherein the logic value stored in the flip-flop corresponds to an output of the flip-flop.

25. (Original) The flip-flop of claim 20, wherein the step of selectively disabling is performed when said mode configuration signal configures the flip-flop in the normal mode of operation.